An Ultra-wideband Low-power Low-noise Amplifier Linearized by Adjusted Derivative Superposition and Feedback Techniques

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***Abstract*—Ultra-wideband (UWB) applications require low-power and low-noise amplifiers (LNAs) that can operate over a wide frequency range. However, conventional LNAs often suffer from poor linearity and high-power consumption. This research work proposes a novel LNA design that uses the adjusted derivative superposition (DS) technique and feedback to improve the linearity and reduce the power consumption of UWB LNAs. The DS technique enhances the third-order intermodulation (IM3) cancellation by adjusting the bias currents of the transistors, whereas the feedback improves the stability and input matching of the LNA. The LNA is implemented using a degenerated common source topology in a 180 nm standard CMOS technology. The simulation results show that the LNA achieves a power gain of 10–12.2 dB, an input third-order intercept point (IIP3) of about 12 dBm, and a noise figure of less than 2.5 dB over the UWB frequency band of 3.1–10.6 GHz. The input reflection coefficient is less than -10 dB, and the power consumption is 11.6 mW with a 1.5 V power supply. The designed LNA offers a novel and innovative solution for UWB applications that significantly improve the performance and efficiency of UWB LNAs whereas reducing the cost and complexity of implementation.**

***Index Terms*—Derivative superposition technique, Low-noise amplifier, Low power, Linearization.**

I. Introduction

One of the frequently used blocks in wireless receiver systems is low-noise amplifiers (LNAs) (Nakhlestani, Hakimi, and Movahhedi, 2012; Hu, et al., 2014; Kim, 2009). There are many technologies to implement the LNAs, such as optical amplifiers (Chaqmaqchee, 2016; Yaba and Chaqmaqchi, 2022) or CMOS technology (Mohebi, et al., 2020). The most important characteristics of the LNAs include low noise, high linearity, and high-power gain. Ultra-wideband (UWB) applications are needed in electronic consumers, such as vehicular radars with high-accuracy operations (Rafati, Qasemi and Amiri, 2019; Kumaravel, et al., 2016; Zhang and Sánchez-Sinencio, 2010; Kazemi and Hayati, 2021; Wang, 2021; Roobert and Rani, 2020). Ultra-wideband systems are approved for use in 3.1–10.6 GHz bandwidth. An ultra-wideband LNA must benefit from appropriate wideband input matching as well as the low and flat noise figure. Power consumption is another major parameter for portable devices to extend the battery lifetime. To decrease the power consumption of the circuit, a simple way is to use a lower supply voltage. Lowering the voltage leads to achieving lower power-consuming circuits (Zhang and Sánchez-Sinencio, 2010; Rastegar and Jee-Youl, 2015; Eskandari, Ebrahimi and Sobhi, 2018; Sahoolizadeh, Jannesari and Dousti, 2018; Huang, et al., 2018). Resistive feedback topology in LNAs delivers suitable input matching, and high-power gain, as well as ultra-wideband operation (Singh, Arya and Komar, 2018; Saberkari, et al., 2016; Kim, et al., 2005). In Gm-boosting technique, the input signal is applied to the gate and source of MOSFET, simultaneously, which has been presented by (Kim and Kim, 2006). It increases the V_{GS} swing whereas it decreases the power consumption and provides a suitable noise figure. However, it is still challenging to achieve a lower than 2 dB noise figure (Hu, et al., 2014). The derivative superposition (DS) method (Aparin and Larson, 2005) is a specific expression of the feed-forward technique, where the main or auxiliary amplifiers are realized with transistors that are operating in distinct regions. In addition, the gate-induced noise of the weak-inversion transistor declines the noise figure. The DS technique complicates input matching (Ganesan, Sánchez-Sinencio, and Silva-Martinez, 2006; Guo and Li, 2013).

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Post-distortion is another technique presented by (Kim, 2009). This method is noteworthy for improving the IP3 and easing input matching (Kim, et al., 2006; Sturm, Popuri and Xiang, 2016). However, the auxiliary amplifier in (Zhang, Fan and Sánchez-Sinencio, 2009) solves problems in canceling the non-linear distortion. Another post-distortion method is introduced for ultra-wideband low-noise amplifiers. Controlling the bias absorbs the second and third-order distortion current over a wide frequency band. This technique improves *IIP2* and *IIP3;* however, it is still challenging to achieve a lower than 2 dB noise figure.

In (Chung, et al., 2015), authors have used the single ended input and diffrential input modes. According to the Capacitive Cross Coupled Dual-Gm-Enhancement architecture, the circuit might be reconfigured as distinct versions of single-ended or differential inputs (Chung, et al., 2015). In single-ended input mode, the noise figure is not sufficient and does not provide wide bandwidth, whereas, in differential input mode, the frequency varies from 1.4 dB to 11.4 dB, which is a good bandwidth. However, achieving flat gain and sufficient linearity is still challenging.

This manuscript is formed as follows: The next part describes the proposed ultra-wideband (UWB) LNA circuit design. In this part, the input matching has been discussed first. Then, gain calculations have been explained. Noise and linearity issues have been described within this part. The simulated results have been provided in the next part. Eventually, an overall conclusion has been presented.

II. Proposed UWB LNA

The step-by-step design procedure for the presented LNA can be followed as:

- Step 1: The transistor size and the bias voltage for the main and the auxiliary transistors have been selected, based on the desired noise figure, gain, linearity, and power consumption of the LNA.
- Step 2: The input and the output matching networks for the LNA have been designed, using the source inductance (L_s), the gate inductance (L_g), the output inductance (L_o), and the output capacitance (L_c). The matching networks are used to match the input and the output impedance of the LNA to the source and the load impedance, which are usually 50 *ohms*. The matching networks also affect the noise figure, the gain, and the stability of the LNA. The matching networks are designed using the Smith chart and the lumped element model. The goal is to minimize the noise figure and maximize the gain and the stability of the LNA over the entire frequency band.
- Step 3: The feedback network for the LNA has been designed, using the feedback resistance (R_f) and the output resistance (R_o). The feedback network is used to provide negative feedback to the LNA, which improves the stability and the linearity of the LNA. The feedback network also affects the gain and the noise figure of the LNA. The feedback network can be designed using the feedback theory and the small-signal model of the device. The goal is to achieve a trade-off between the stability, the linearity, and the gain of the LNA.
- Step 4: The performance of the LNA has been simulated and verified, using the pre-layout and post-layout simulation tool, respectively. The simulation and verification are used to check if the LNA meets the design specifications and the quality standards.

Between different linearization methods, derivative superposition (DS) and feedback techniques have been adjusted and applied to improve the linearity. This technique is called "derivative superposition" since it adds the third-order derivative of g_3 of the drain current to cancel the distortion. Both transistors biased in weak and strong inversion regions are used, respectively. The auxiliary transistor produces a positive third-order derivative of g_3 to cancel the negative g_3 of the main MOSFET. Thus, the linearity is increased within a full dc performance limit. However, second-order interaction at high frequencies often limits the effect. The DS technique reduces major issues whereas it entangles input matching (Aparin and Larson, 2005). For designing the low-noise amplifier, a common-source amplifier is used for the input stage. The proposed UWB LNA has been illustrated in Fig. 1.

In common source, the gate-drain capacitor can be considered as a Miller feedback capacitor so that it causes the loading effect on input matching. In fact, in low frequencies, the gate-drain capacitor acts like negative feedback, and whereas most of the loads are inductive, an inductor in the source of the transistor is applied to reduce the input inductive loading effect. This method is called source degeneration. As mentioned before, positive a third-order derivative of g_3 from the auxiliary transistor cancels the negative term created by the main transistor. The values of different parameters of the proposed LNA have been illustrated in Table I.

A. Input Matching

In the design of low-noise amplifiers, common gate or common source is used for the input stage. In ultra-wideband applications, usually, the best choice is common gate which provides a wide bandwidth (Kumar and Kumar Deolia, 2019). As shown in Fig. 2, there is Miller's effect in the common source, whereas in the common gate, Miller's effect does not exist. Miller's effect in the gate-drain capacitor makes the total capacitance connected to the gate increased so that the inverse relation between f_t and the capacitors connected to the gate causes a decrement in f_t of the transistor.

In source degeneration, an inductor in the gate of the transistor has been put to adjust input matching to reduce L_s. Thus, the input impedance seen in source resistance is:

$$Z_{in} = s\left(L_S + L_g\right) + \frac{1}{sC_{gs}} + \frac{L_S g_{ma}}{C_{gs}} \quad (1)$$

The inductor placed in the source of the transistor provides a real part in the input so that if this real part will be equated with source impedance, a proper input matching will be achieved. By neglecting the channel length modulation, total input impedance consists of two transfer zeros and a pole at the origin that is explained below:

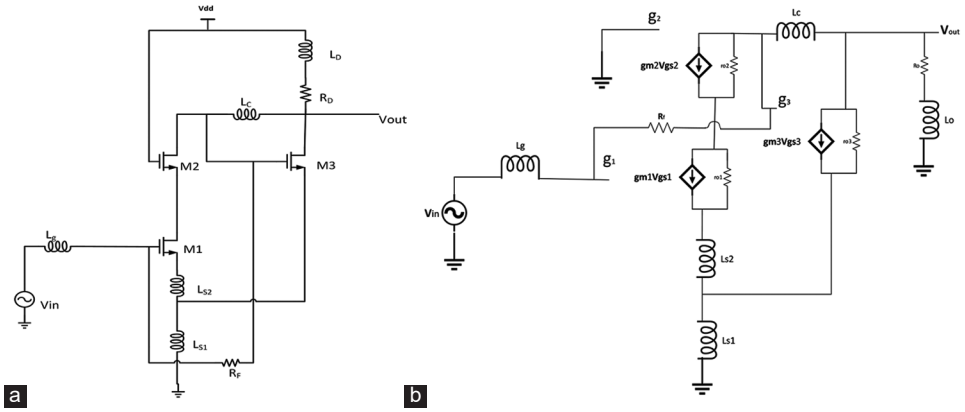

Fig. 1. A complete scheme and small signal equivalent circuit of proposed ultra-wideband (a) complete scheme (b) small signal equivalent circuit.

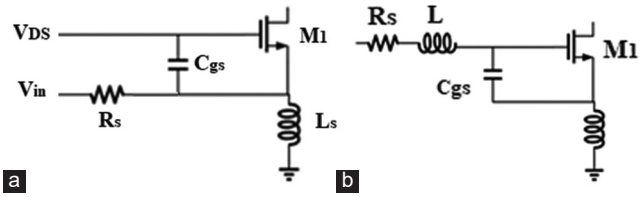

Fig. 2. The input stage (a) without the Miller effect (b) with the Miller effect.

$$Z_{in} = \frac{S^2 + S\dfrac{g_{m1}L_s}{(L_s+L_g)C_{gs1}} + \dfrac{1}{(L_s+L_g)C_{gs1}}}{S/(L_s+L_g)} \quad (2)$$

As known, the real part is strongly dependent on variations of transistor length/width and inductor. This point causes sensitivity increment on the variation of the parameters that reduce input matching bandwidth. Finally, a new technique has been suggested to solve this problem. As shown in Fig. 3, any inductor value increment increases the real part. As seen in the figure, the most optimized inductor value has been chosen between 0.2 and 0.5 nH. Furthermore, frequency increment causes a reduction in the real part so that the gate-source capacitance can be controlled by L_g variations, but the imaginary part is increased by L_s and frequency increment; this makes the circuit inductive. However, the effect of the noisy gate-source capacitor increases by frequency increment so that the circuit treats like a capacitor at frequencies up to 10 GHz. Ω

At the frequency of 9 GHz, the real and imaginary parts are in the best condition, but whereas the good input matching should be <−10 dB, this situation achieves 0.2 to 0.5 nH. The input matching is calculated as follows:

$$S_{11} = \frac{Z_{in}-Z_s}{Z_{in}+Z_s} = \frac{1+s^2C_{gs}(L_g+L_s)+sg_mL_s-sR_sC_{gs}}{1+s^2C_{gs}(L_g+L_s)+sg_mL_s+sR_sC_{gs}}$$

$$= \frac{1+s^2C_{gs}(L_g+L_s)}{1+s(g_mL_s+R_sC_{gs})+s^2C_{gs}(L_g+L_s)} \quad (3)$$

Whereas the input matching has an inverse relation with the bandwidth, it does not provide enough bandwidth, so the quality factor to achieve input matching should be reduced in an ultra-wideband frequency. An R_f resistor can be used to improve input matching as seen in Fig. 4, although it reduces the gain.

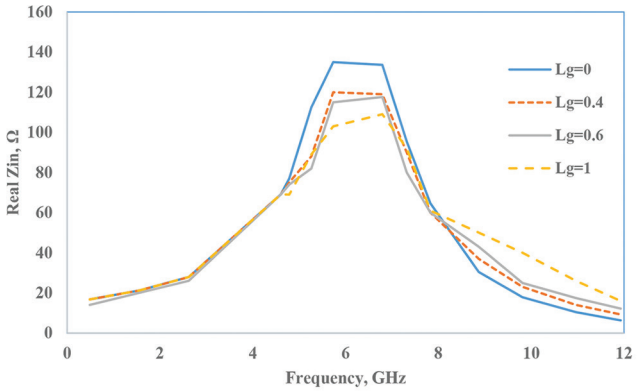

Fig. 3. The plot of real part variation for different L_g.

TABLE I
VALUES OF DIFFERENT PARAMETERS OF THE PROPOSED LNA

Parameter	Value	Parameter	Value
$\left(\frac{w}{L}\right)_{M_1}$	$\frac{320\,\mu m}{180\,nm}$	L_{s1}	0.05 nH
$\left(\frac{w}{L}\right)_{M_2}$	$\frac{320\,\mu m}{180\,nm}$	L_{s2}	0.29 nH
$\left(\frac{w}{L}\right)_{M_3}$	$\frac{230\,nm}{180\,nm}$	L_g	0.48 nH
V_{dd}	1.5 V	L_o	5.04 nH
R_o	9.42 Ω	L_c	1.19 nH
r_{o1}	25.62 Ω	r_{o2}	34.47 Ω
R_f	3.39 KΩ	gm^1	0.018 A/v
gm^2	0.018 A/v	R_s	50 Ω

$$S_{11} = \frac{Z_{in}-Z_s}{Z_{in}+Z_s} = \frac{1+s^2C_{gs}(L_g+L_s)}{1+s\left(\dfrac{R_fg_mL_s}{g_mL_s+R_fC_{gs}}+R_s\right)+s^2C_{gs}(L_g+L_s)}$$

$$= 20\log\left(\left|\frac{3f^2}{62500f\times i\text{-}3f^2+1250}\right|\right) \quad (4)$$

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Hence, the input matching is expressed as follows:

$$Q_{in} = \frac{1}{\omega CR} = \frac{1}{\omega C_{gs}(R_s + g_m L_s / C_{gs})}$$
$$= \frac{1}{\omega(R_s C_{gs} + g_m L_s)} = \frac{1}{2\omega R_s C_{gs}} \quad (5)$$

$$\omega_0{}^2 = \frac{1}{(L_s + L_g)C_{gs}} \cdot Q = \frac{1}{2R_S \omega_0 C_{gs}} \quad (6)$$

B. Gain Analysis

Whereas R_f is used in the feedback form to achieve full input matching, it reduces the gain. Furthermore, adding transistor M_2 causes a limited increment in the gain, but as known, M_2 noisy gate-drain capacitor reduces bandwidth by adding a dominant pole. Inductor *Lo* is used to improve the gain. The effect of *Lo* on the gain is shown in Fig. 5.

Calculating total gain with channel length modulation neglecting the M_1 gate capacitor is:

$$G_{eff}(S) = \frac{I_{out}}{V_s} = \frac{g_m}{(R_s + Z_{in})sC_{gs}}$$
$$= \frac{g_m}{1 + s\left(\frac{R_f g_m L_s}{g_m L_s + R_f C_{gs}} + R_s\right)sC_{gs+s^2 C_{gs}(L_g + L_s)}} \quad (7)$$

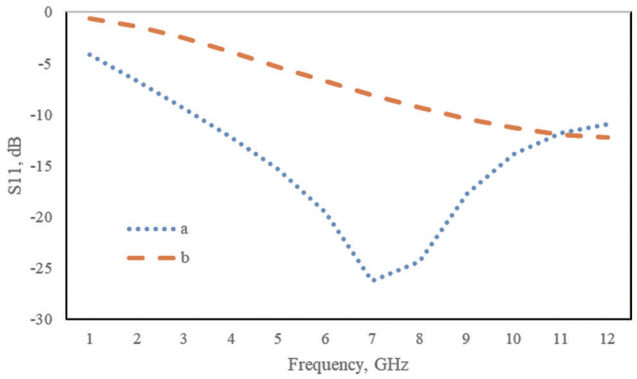

Fig. 4. The plot of S_{11} (a) with R_f (b) without R_f.

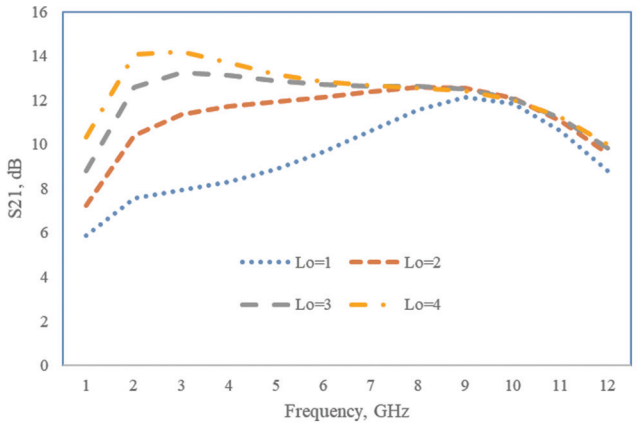

Fig. 5. The plot of S_{21} variation for different L_o (nH).

$$G = G_{eff} = \sqrt{\frac{g_m^2}{[1-\omega^2 C_{gs}(L_g + L_s)]^2 + \omega^2\left(\frac{R_f g_m L_s}{g_m L_s + R_f C_{gs}} + R_s\right)^2}} \quad (8)$$

$$S_{21} = 2G_{eff} R_L = \frac{2g_m R_D 20}{+s\left(\frac{R_1 g_m L_s}{g_m L_s + R_f C_{gs}} + R_s\right)}\Bigg|_{\omega=\omega_0}$$
$$= 20\log\left(\left|\frac{1\text{-}2.76333\times10^{-29}\ f^2}{1+(f(2.63\times10^{-14}\ i)\text{-}2.76333\times10^{-29}\ f)}\right|\right) \quad (9)$$

This pole that is created in high frequency must be shifted to the right (reducing capacitive effect), so the best choice for getting this pole away is using L_c. The effect of the variation of *Lc* on bandwidth is shown in Fig. 6.

The voltage gain of the LNA is easily obtained as follows:

$$G_m = \frac{I_{out}}{V_s} = \frac{r_{o2} - \frac{g_{m1}R_1(1+g_{m2}r_{o2})}{\frac{1}{r_{o1}} + \frac{1}{ro2} + g_{m2}}}{r_{o2}(R_1 + R_2)} \quad (10)$$

If $g_{m1}r_{o1} \gg 1$ then $\quad r_{o2} \ll r_{o1}(1 + g_{m2}r_{o2})$

$$G_m \cong \frac{g_{m1}R_1}{(R_1 + R_s)} \quad (11)$$

$$R_{out} = [R_D \| (R_1 + R_S) \| (r_{o2} + (1 + g_{m2}r_{o2})r_{o1})] \quad (12)$$

$$A_V = G_m R_{out} \text{ (Aparin and Larson, 2005)} \quad (13)$$

C. Noise Analysis

In the proposed LNA, there are four different noise sources consisting of M_1, M_2, $_{R1}$, and $_{RD}$. M_3 noise and gate noise current have been neglected whereas the transistor is biased in the triadic region (Fig. 7).

Noise of $M_{1:}$

$$\frac{V_1}{R_s} + \frac{V_1}{R_1} = 0 \rightarrow V_1 = 0 \quad (14)$$

$$I_{nM1+}\frac{V_2}{r_{o1}} + \frac{V_2}{r_{o2}} + g_{m2}V_2 = 0 \quad (15)$$

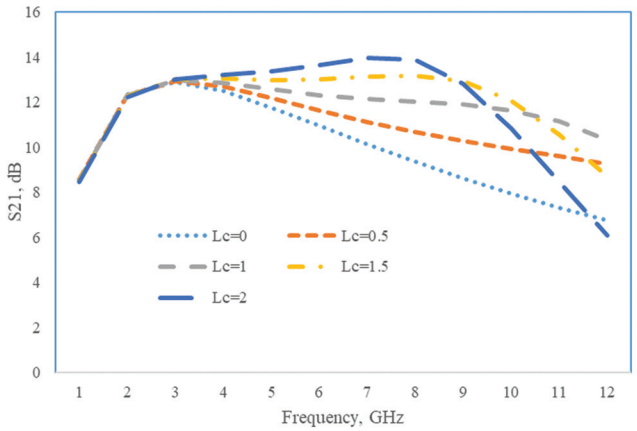

Fig. 6. The plot of S_{21} variation for different values of L_c (nH).

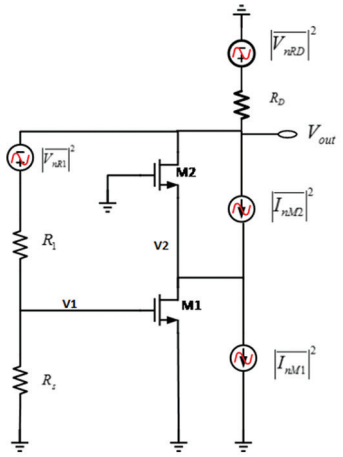

Fig. 7. Equivalent noisy circuit of the proposed low-noise amplifiers.

$$V_2 = \frac{-I_{nM1}}{\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + g_{m2}} \tag{16}$$

$$I_{out} = g_{m2}V_2 + \frac{V_2}{r_{o2}} \tag{17}$$

$$I_{out} = -\frac{1+g_{m2}r_{o2}}{r_{o1}} \frac{I_{nM1}}{\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + g_{m2}} \tag{18}$$

Considering $g_{m2}r_{o2} \gg 1$ and $r_{o2} \ll r_{o1}\left(1+g_{m2}r_{o2}\right)$

$$I_{out} \cong \frac{r_{o2}}{r_{o1}} I_{nM1} \tag{19}$$

According to the above calculations, the noise of M_1 is shown in equation (20):

$$F_{M1} = [\frac{r_{o2}}{r_{o1}}\left(1+\frac{R_s}{R_1}\right)]^2 \frac{\gamma}{g_{m1}R_s} \tag{20}$$

The channel length modulation M_1 must be reduced to reduce the input transistor noise effect in the output.

Noise of M_2:

$$g_{m2}V_2 + \frac{V_2}{r_{o1}} + \frac{V_2}{r_{o2}} + I_{nM2} = 0 \tag{21}$$

$$I_{out} = g_{m2}V_2 + I_{nM2} + \frac{V_2}{r_{o2}} \tag{22}$$

$$I_{out} = -\frac{V_2}{r_{o1}} \tag{23}$$

$$V_2 = \frac{-I_{nM2}}{\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + g_{m2}} \tag{24}$$

$$I_{out} = \frac{I_{nM2}}{1+\frac{r_{o1}}{r_{o2}} + g_{m2r_{o1}}} \tag{25}$$

$$-r_{o1}I_{out} = \frac{-I_{nM2}}{g_{m2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}}} \tag{26}$$

Considering $g_{m2}r_{o2} \gg 1$, noise of M_2 is shown in equation (27):

$$F_{M2} = \frac{\gamma}{(g_{m1}g_{m2}r_{o1})^2}(1+\frac{R_S}{R_1})^2 \tag{27}$$

Noise of R_1

$$V_1 = \frac{R_s}{R_1+R_2} V_{nR1} \tag{28}$$

$$g_{m1}V_1 + \frac{V_2}{r_{o1}} + \frac{V_2}{r_{o2}} + g_{m1}V_2 = 0 \tag{29}$$

$$I_{out} = -\frac{V_{nR1}}{R_1+R_2} + g_{m2}V_2 + g_{m2}V_2 + \frac{V_2}{r_{o2}} \tag{30}$$

$$r_{o2}I_{out} = -\frac{r_{o2}}{R_1+R_2}V_{nR1} + \left(g_{m2}r_{o2}+1\right)V_2 \tag{31}$$

$$V_2\left(\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + g_{m2}\right) = -\frac{g_{m1}R_s}{R_1+R_2}V_{nR1} \tag{32}$$

$$r_{o2}I_{out} = -\frac{r_{o2}}{R_1+R_2}V_{nR1} - \left(1+g_{m2}r_{o2}\right)$$

$$\left(\frac{\frac{g_{m1}R_s}{\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + g_{m2}} \frac{1}{R_s+R_1}}{}\right) V_{nR1} \tag{33}$$

$$r_{o2}I_{out} = -\frac{V_{nR1}}{R_1+R_2}V_{nR1} - \left(r_{o2} + \frac{g_{m1}R_s\left(1+g_{m2}r_{o2}\right)}{\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + g_{m2}}\right)V_{nR1} \tag{34}$$

$$I_{out} = (\frac{1-g_{m1}R_s}{R_1+R_s})V_{nR1} \tag{35}$$

If $g_{m1}R_s \succ\succ 1$ then:

$$F_{R1} = \frac{R_s}{R_1} \tag{36}$$

The noise of R_1 motivates M_2. To reduce the effects of the output noise of R_1, M_1, and M_2, channel length modulation must be reduced and increased, respectively. This is the same way to reduce the noise of M_1 and M_2 at the output. Hence, the noise of R_1 reduces by M_1 and M_2 noise decrement spontaneously. Furthermore, the value of R_1 must be bigger than the source resistance to decrease noise effects in output.

Noise of R_d:

The noise of R_d directly appears in the output, so the noise figure is:

$$F_{RD} = \frac{(1+\frac{R_S}{R_1})^2}{g_{m1}{}^2 R_D R_S} \tag{37}$$

$$NF = \frac{f^{3.5}}{3.4\times10^3} + 1 \tag{38}$$

D. Linearity

Among different linearization techniques, the derivative superposition (DS) and feedback are chosen to improve linearity.

Whereas source degeneration has two different effects, the increment of linearity by $(1+g\omega L_s)^{3/2}$ and decrement of it, originated from second-order interactions, a technique is explained to reduce second-order interactions in the rest. Furthermore, a feedback has been used to improve the linearity. For *IIP3* (Jafari and Yavari, 2015):

$$A_{IIP3,amplifier} = \sqrt{\frac{4}{3}\left|\frac{g_1}{g_3}\right|} \quad \text{(Jafari and Yavari, 2015)} \tag{39}$$

$$A_{IIP3,closeloop} = \sqrt{\frac{4}{3}\left|\frac{b_1}{b_3}\right|} = \sqrt{\frac{4}{3}\frac{g_1}{g_3}\frac{(1+T_0)^3}{(1-\frac{2g_2^2}{g_1 g_3}\frac{T_0}{1+T_0})}} \tag{40}$$

Negative feedback improves *IIP3* by $(1+T_0)^{3/2}$, where $T_0=g_1\beta$ is the linear feedback factor.

If $g_2 \neq 0$ then IIP3 decreases, LNA non-linearity originates from two primary sources:

The other used technique to improve linearity is utilizing the auxiliary transistor in the triode region that is connected with the main transistor. As known, the non-linear relation of a transistor is defined as:

$$i_{ds} = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 \tag{41}$$

$$g_1 = \frac{\partial I_{DS}}{\partial V_{GS}} \quad g_2 = \frac{\partial^2 I_{DS}}{\partial V^2_{GS}} \quad g_3 = \frac{\partial^3 I_{DS}}{\partial V^3_{GS}} \tag{42}$$

Where g_1, g_2, and g_3 are the linear gain, the second-order, and the third-order non-linearity factors, respectively.

The g_1 and g_2 are both positive but g_3 is negative, then the reduction of g_3 is the goal of linearity improvement. To achieve this goal, an auxiliary transistor has been used in the triode region whereas creating positive g_3. By paralleling transistors, the third-order non-linear factor is reduced.

If $g_{mb} >> C_{gsb}$, the non-linear effects of M_2 can be neglected. The presented LNA linearity equivalent circuit is shown in Fig. 8.

The inductor in the source causes second-order interactions. To solve this problem, the source inductor was divided into two sections. This technique is called Modified Derivative Superposition. When there is no inductor in the source, the vector block diagram is Fig. 9:

However, by placing an inductor in the source, the block diagram is Fig. 10:

By breaking the inductor placed in the source of the transistor, a third-order non-linear factor angle can be easily chosen to neutralize the second-order interaction factor using L_{s2}.

The Volterra series has been applied to analyze linearity. First, some variables must be defined:

$$I_{m1} = g_{m1} V_{gs1} + g_{m2} V_{gs1}^2 + g_{m3} V_{gs1}^3 \tag{43}$$

Whereas transistor M_3 is in the triode region, the first and second-order currents are neglected.

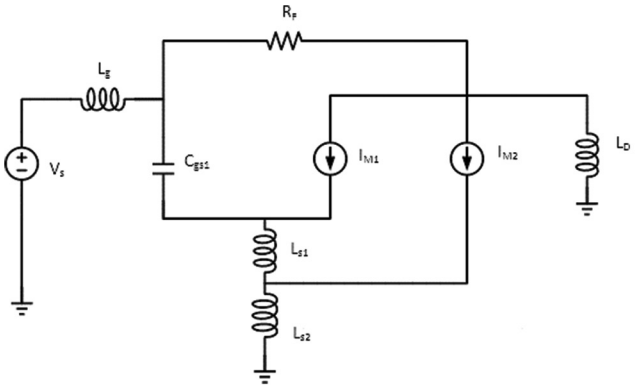

Fig. 8. The linearity equivalent circuit of the proposed low-noise amplifiers.

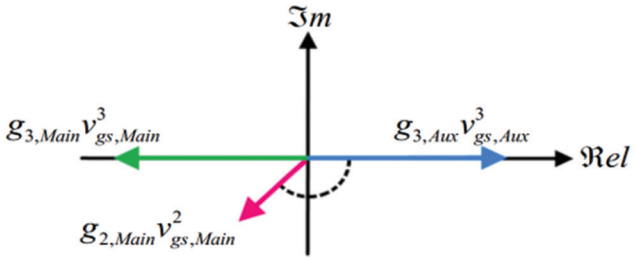

Fig. 9. The vector block diagram without the inductor in the source.

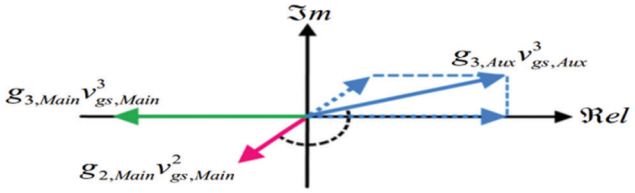

Fig. 10. The vector block diagram with the inductor in the source.

$$I_{out} = A_1 V_s + A_2 V_s^2 + A_3 V_s^3 \tag{44}$$

where:

$$A_1 = \frac{1+\left[sR_f C_{gs1} - \left(R_f + sL_g\right)\left(g_{m1} + sR_f C_{gs1}\right)\right]B_1}{R_f + s\left(L_g + L_D\right)} \tag{45}$$

$$A_2 = \frac{sR_f C_{gs1} B_2 - sL_D A_2}{R_f + sL_g} - \left(g_{ma1} B_2 + g_{ma2} B_1 B_1\right) - sR_f C_{gs1} B_2 \tag{46}$$

$$A_3 = \left(\frac{sR_f C_{gs1}}{R_f + sL_g} - g_{ma1}\right) B_3 - \left(2g_{ma2} B_1 B_2 + g_{ma3} B_1 B_1 B_1\right) - g_{mc3} C_1 C_1 C_1 \tag{47}$$

III. Simulation and Post-layout Results

The presented UWB-LNA has been designed with a 180 nm standard CMOS technology model. The LNA has

been worked under a power supply of 1.5 V. The ADS and Cadence software were used for designing, simulations, pre-layout, and post-layout of the proposed LNA.

The design of the LNA aimed to achieve low-noise figure (NF) and high third-order intercept point (IIP3), which are important parameters for the performance and linearity of the amplifier. The simulated gain (S_{21}) of the LNA across the frequency range of 3.1 to 10.6 GHz is depicted in Fig. 11 which varies from 10 dB to 12.2 dB at this frequency range. The primary goals in the design of the LNA were to improve NF and IIP3. The figure shows that the LNA provides a consistent and flat gain of about 10–12.2 dB over the entire bandwidth, which is desirable for wideband applications. The NF of the LNA, which measures the amount of noise added by the amplifier to the input signal, is presented in Fig. 12. The figure demonstrates that the LNA exhibits a very low NF of 1.5–2.5 dB within the operating frequency band, which indicates a high signal-to-noise ratio (SNR) at the output. The IIP3 of the LNA, which measures the ability of the amplifier to handle large input signals without distortion, is displayed in Fig. 13. The figure reveals that the LNA achieves a high IIP3 of about 10 dBm at the center frequency of 6.85 GHz, which implies a good linearity and dynamic range for the amplifier. The input reflection coefficient (S_{11}) of the LNA, which measures the degree of impedance matching between the amplifier and the source, is illustrated in Fig. 14. The figure indicates that the LNA has a low S_{11} of less than -10 dB over the entire frequency band, which means that most of the input power is delivered to the amplifier and the reflection is minimized. The stability factors (K and Delta) of the LNA, which measures the tendency of the amplifier to oscillate, are shown in Fig. 15. The figure confirms that the

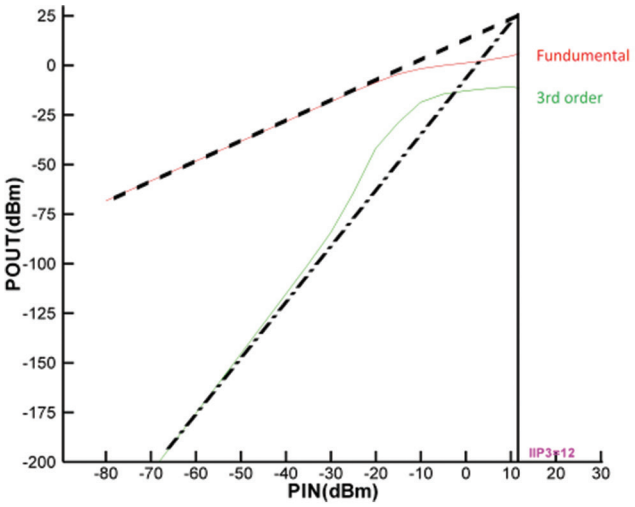

Fig. 13. The *IIP3* of the proposed CMOS low-noise amplifiers.

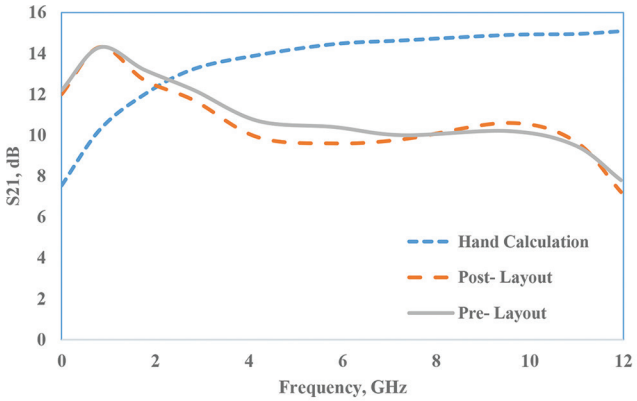

Fig. 11. The S_{21} parameter.

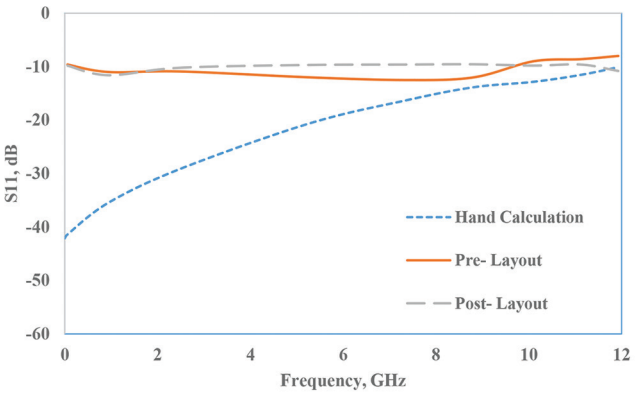

Fig. 14. The S_{11} parameter.

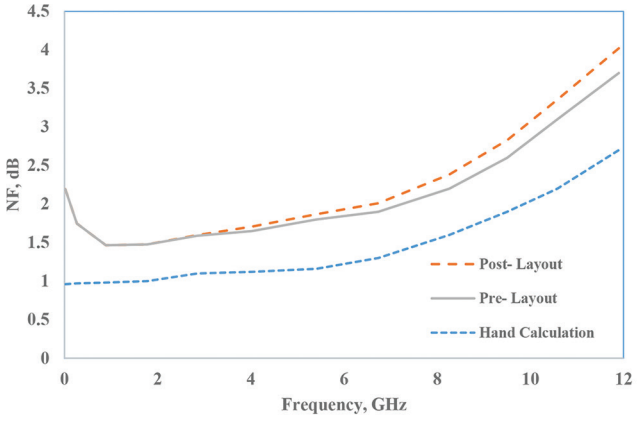

Fig. 12. The noise figure

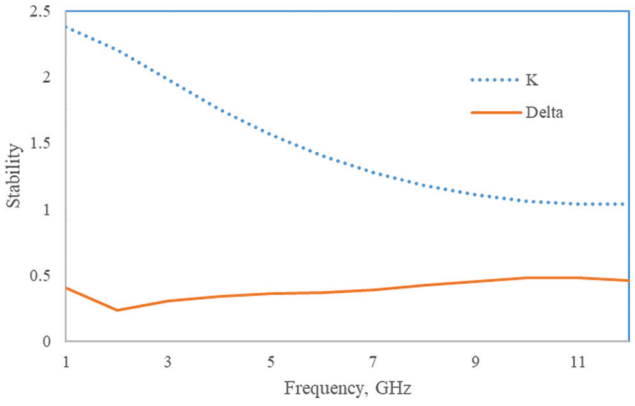

Fig. 15. The stability factor.

 http://dx.doi.org/10.14500/aro.11267

TABLE II
PERFORMANCE COMPARISON OF THE PROPOSED LNA WITH SIMILAR WORKS

Ref.	*Tec* (nm)	*Results type*	*BW* (GHz)	S_{11} (dB)	S_{21} (dB)	NF_{min} (dB)	*Pdc* (mw)	*IIP3* (dBm)
Rafati, Qasemi and Amiri, 2019	130	Post-layout	3.1–10.6	<–10	12	1.8	11.2	13.8
Kumaravel, et al., 2016	180	Post-layout	2.44	–15	14.6	2.9	3.8	4.19
Rastegar and Jee-Youl, 2015	130	Pre-layout	3.1–10.6	NA	10.24	0.9	17.92	6.8
Eskandari, Ebrahimi and Sobhi, 2018	180	Post-layout	0.6–3.15	–13	20.2	3.1	6	–2.1
Sahoolizadeh, Jannesari and Dousti, 2018	130	Post-layout	3.1–4.8	<–10	15.8	1.7	11.28	8.32
Huang, et al., 2018	180	Post-layout	3–3.5	<–10	14.6	2.9	14.8	1.2-4.7
Kazemi and Hayati, 2021	180	Post-layout	3.1–10.6	–11	15.6–16.5	2.2–3	6.8	–4
Hayati, et al., 2020	180	Post-layout	3–10.6	<–10	12.79	2	11.56	–8
Kazemi and Hayati, 2021	180	Post-layout	1–8	–11	14.7–15.4	2.3–4.4	5.4	2.7
This work	180	Post-layout	3.1–10.6	<–10	10-12.2	1.5–2.5	11.6	12

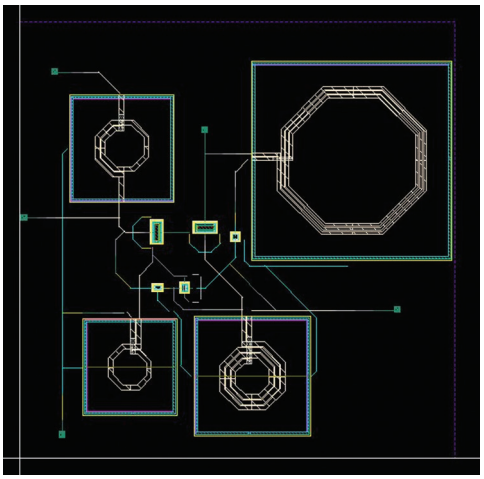

Fig. 16. The layout of the low-noise amplifiers.

LNA has a K value of greater than one for all frequencies, which ensures that the amplifier is unconditionally stable and does not generate any unwanted oscillations.

The characteristics of the proposed ultra-wideband LNA have been compared with similar published articles, as can be seen in Table II. Moreover, as shown in the physical layout in Fig. 16, the presented LNA occupies a 0.58 mm × 0.7 mm chip area.

A figure of merit (FOM) factor has been defined by (Zhang and Sánchez-Sinencio, 2010) to cover all important characteristics of an ultra-wideband LNA as below:

$$FOM = \frac{IIP3[mW] \times Gain[abs] \times BW[GHz]}{P_{dc}[mW] \times (F-1)}$$ (Zhang and Sánchez-Sinencio, 2010) (48)

Where IIP3 is the maximum value for third-order input intercept point, gain has been considered as the maximum power gain in magnitude; BW covers the -3-dB bandwidth; P_{dc} has been set as the power dissipation; and (F-1) has been considered as the minimum excess noise figure in magnitude. FOM of this work is equal to 83.3.

IV. Conclusion

In this paper, both the adjusted derivative superposition technique and the feedback technique have been used to improve linearity since using the feedback technique alone was not enough. An auxiliary transistor that is biased in the deep triode region was connected with the main transistor, generates positive g_3, and improves linearity. An inductor in the source is divided into two parts to change phase direction. In this LNA, very low-noise and low-power consumptions have been achieved. Furthermore, the gain, linearity, and input matching are adjusted in a suitable range.

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