http://dx.doi.org/10.14500/aro.12810

A 5G Doherty Power Amplifier Design Using Two-Section Impedance Transfer Networks

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***Abstract*–This paper introduces a simulation-based design study of a high-performance 2.6 GHz Doherty power amplifier (DPA) designed for 5G New Radio n7 and n38 frequency band applications. The proposed DPA incorporates a branch-line coupler, replacing conventional impedance inverter and impedance transformer networks. Furthermore, an innovative compact two-section impedance matching network is incorporated in the amplifier structure to reduce size and improve performance. This novel approach results in superior performance, particularly at high output power levels. A class-AB amplifier serves as the main stage, whereas a class-C amplifier functions as the auxiliary stage, ensuring efficient power utilization. Operating at 2.6 GHz, the proposed DPA demonstrates a drain efficiency of 45% and a maximum gain of 15 dB. In comparison with a typical DPA, the proposed design occupies 75% of the size, which shows a size reduction of 25%.**

***Index Terms*—5G new radio applications, Branch-line coupler, Compact design, Doherty power amplifier, Matching networks, Power efficiency.**

I. Introduction

The rapid increase in power consumption of wireless devices can be attributed to the escalating demand for higher data rates, alongside the growing number of wireless communication users (Ahmed, et al., 2021, Lu, et al., 2025). To mitigate power losses, enhancing the efficiency of base stations is imperative. Improving the efficiency of power amplifiers (PAs) deployed in base stations yields substantial energy savings for RF transmitters (Xiao and Zhang, 2025). Various techniques have been explored to enhance the efficiency and linearity of PAs, including Doherty amplifiers (Doherty, 1936, Chen, et al., 2025), envelope tracking (ET) (Varma, et al., 2025, Bo, et al., 2025), and varactor-based dynamic load modulation (Nemati, et al., 2009, Turalchuk, Filipiuk and Iskakov, 2024). Among these methods, the Doherty PA (DPA) stands out due to its simple structure and configuration, offering several advantages. Furthermore, the DPAs provide higher output power, higher average efficiency, and wider modulated bandwidth, compared to similar PA structures (Camarchia, et al., 2015).

The concept behind the DPA involves modulating the output load of a main active device using the generated current of an auxiliary active device (Colantonio, et al., 2009, Giofre, et al., 2013). To facilitate active load modulation effectively, an impedance inverter network (IIN) is positioned between the main device and the output load. In addition, to match the standard output termination to the DPA, an impedance transforming network (ITN) is necessary (Colantonio, et al., 2009). Typically, both the impedance transformer network (ITN) and IIN in the standard DPA are implemented using a quarter-wave transmission line (λ/4-TLine) (Nikandish, Staszewski and Zhu, 2020, Zhou, et al., 2020).

Recent studies have shown improvements in DPA performance by optimizing the output combiner (Liu and Wang, 2024, Hussein, et al., 2025), whereas others have focused on enhancing the amplifiers' output matching networks (Yang and Ke, 2025, Zhang, et al., 2024). Alternatively, in (Choi, 2023, Huang and Liu, 2024, Spagnolo,

ARO-The Scientific Journal of Koya University
Vol. XIV, No.2 (2026), Article ID: ARO.12810. 52 pages
DOI: 10.14500/aro.12810
Received: 31 December 2025; Accepted: 07 August 2026
Regular research paper; Published: 17 September 2026
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2025), techniques such as lumped reactive components and defected ground structure (DGS) have been employed for harmonic suppression in DPAs, albeit requiring an extra fabrication process, which is undesirable for low-cost, mass production environments. Recently, resonators have gained popularity in power dividers to suppress harmonics and reduce device size, suggesting their potential application in DPA design for similar purposes (Roshani, et al., 2023; MahdiAbadi, et al., 2024, Mezaal, Ghazi and Khaleel, 2025, Al-Majdi and Mezaal, 2023).

In the proposed paper, a simulation-based design study of DPA is presented, in which the conventional IIN and ITN are replaced by a branch-line coupler and the conventional matching network is replaced by two-section matching networks. The steps of the design process of the proposed DPA are illustrated in Fig. 1. As shown, in step 1, the DPA specifications such as operating frequency and output power are considered. In the second step, the design starts from the initial DPA structure. Then, in steps 3 and 4, the proposed coupler structure is extracted, and in steps 5 and 6, the two sections' input and output impedance transformers are designed. These steps are explained in detail in the next sections.

A. Research Gap and Novel Contributions

Despite the important progress reported in previous DPA designs, a clear challenge still remains. Many existing approaches improve efficiency, output combining, or harmonic control, but they often use conventional impedance matching networks or additional techniques that increase circuit complexity, occupied area, or fabrication effort. Therefore, there is still a need for a compact and practical DPA structure that can provide high efficiency and acceptable linearity without relying on extra fabrication steps or bulky matching sections. In this work, this gap is addressed using a branch-line coupler as the main combining structure together with a compact two-section matching network, aiming to simplify the architecture while reducing size and preserving strong RF performance.

Previous studies have provided important foundations for the design of DPAs and impedance matching networks. (Giofre, et al., 2013) presented an important output combining approach for DPAs, in which the functions of the impedance inverting network and the impedance transformer network are integrated into a single output combining structure. This approach helps to obtain more practical transmission-line impedances and simplifies the output network, especially in high-power DPA designs. In addition, (Chen and Hamid, 1987) provided a theoretical method for designing two-section impedance transformers with arbitrary electrical lengths, which is useful for transforming complex impedances in microwave circuits.

The novelty of the proposed structure lies in the compact integration of two established design concepts within a 2.6 GHz DPA architecture. Specifically, the design employs a branch-line coupler to replace conventional impedance inverter and impedance transformer networks, together with a compact two-section impedance matching network for practical impedance transformation. Unlike (Chen and Hamid, 1987), which mainly provides the theoretical basis for two-section impedance transformers, and unlike (Giofre, et al., 2013), which focuses mainly on the Doherty output combining concept, the present work integrates these ideas into a compact simulation-based DPA design.

II. Theoretical Analysis and Design Equations

Fig. 2 shows the block diagram of the proposed DPA amplifier, which explains the entire architecture. The proposed structures of the input branch-line coupler, input impedance transformer network, output impedance transformer network and output branch-line coupler are illustrated. The design equations of these blocks are extracted and explained in this section.

Fig. 3a illustrates the IIN and ITN for a standard DPA. In this configuration, the main and auxiliary amplifiers are connected via a quarter-wave transmission line. In the designed structure, the output coupler is applied instead of the IIN and ITN networks based on the proposed technique in (Giofre, et al., 2013). As shown in Fig. 3b, the coupler is composed of four quarter-wave (λ/4) transmission lines. The horizontal λ/4

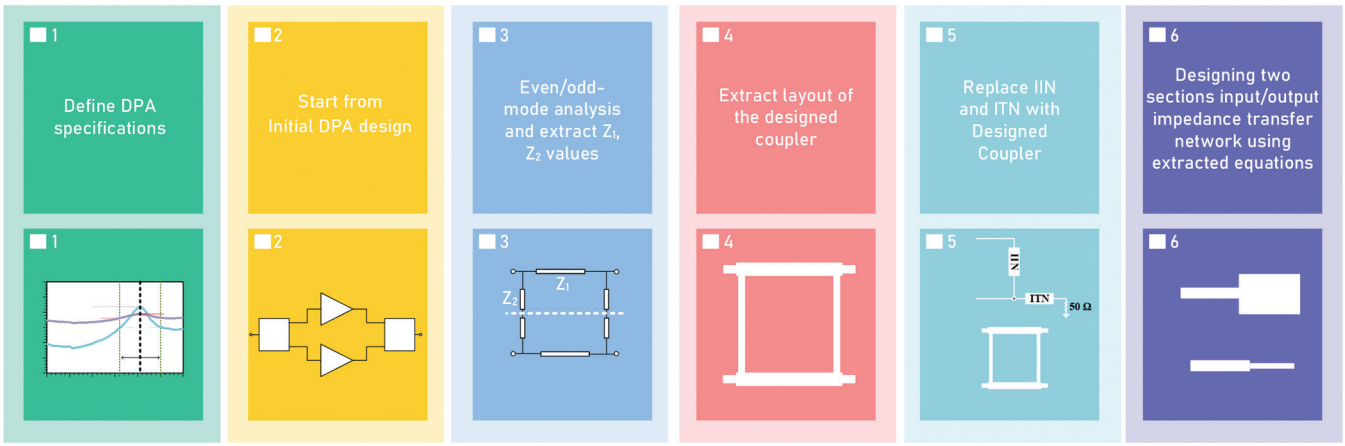

Fig. 1. Design procedure of the proposed Doherty power amplifier, which is explained in six steps.

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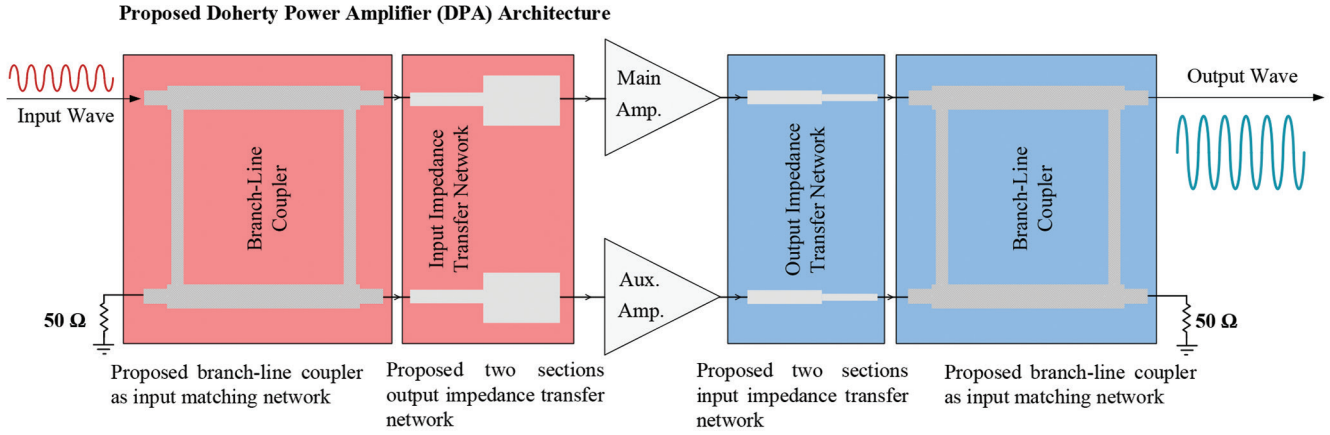

Fig. 2. Block diagram of the proposed Doherty power amplifier.

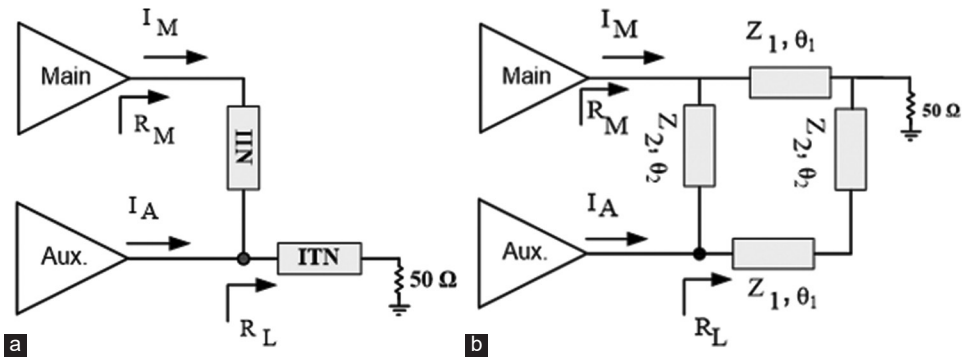

Fig. 3. (a) Conventional and (b) modified Doherty power amplifier combiner implementation.

transmission lines have equal impedance (Z_1), and the vertical λ/4 transmission lines have equal impedance (Z_2).

A. Power Combining Network

A power combiner is an influential component in the DPA's structure. A branch-line coupler is used in the proposed DPA as a power combiner network. Fig. 4 shows the structure of the branch-line coupler, consisting of four quarter-wave transmission lines.

The schematic diagrams of the even- and odd-mode for the branch-line coupler are shown in Fig. 5a and b, respectively.

To avoid any ambiguity, the symbols used in this section are defined here. Z_{ein} and Z_{oin} are the input impedances seen under even-mode and odd-mode operation, respectively. Z_{ein1}, Z_{ein2}, Z_{oin1}, and Z_{oin2} are the impedances appearing in the intermediate steps of the equivalent-circuit analysis. Z_{S2} and Z_{L2} are the target source impedance and load impedance at the impedance transformer network. The terms (Z_1, θ_1) and (Z_2, θ_2) indicate the impedances and electrical lengths of the transmission-line sections used in the design.

The admittance Y_{out} shown in Fig. 6 is obtained from (1) (Monzon, 2002).

$$Y_{out} = \frac{Z_i + jR\tan\theta_i}{RZ_i + jZ_i^2\tan\theta_i} \quad (1)$$

According to Fig. 5a, under even mode excitation, R = ∞, so from (1), Y_e is expressed as follows:

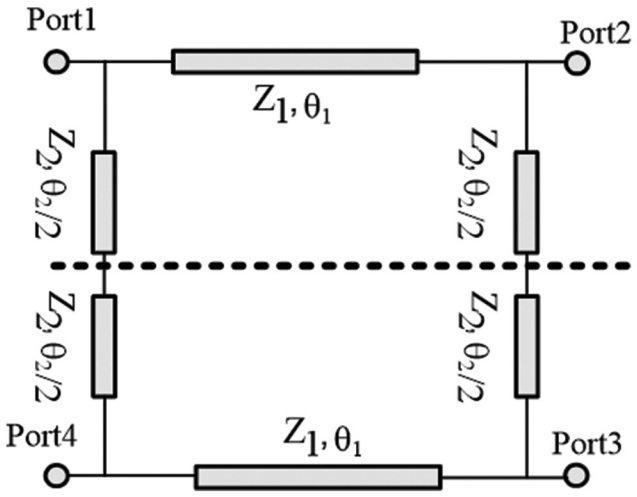

Fig. 4. Schematic diagram of the coupler.

$$Y_e = \frac{jR\tan\theta_i}{RZ_i} = \frac{j\tan\theta_i}{Z_i} \quad (2)$$

Therefore, Z_e is equal to:

$$Z_e = -jZ_i \cot\theta_i \quad (3)$$

According to Fig. 5b under odd mode excitation, R= 0; hence, from (1), Y_o is expressed as follows:

$$Y_o = \frac{Z_i}{jZ_i^2\tan\theta_i} = \frac{1}{jZ_i\tan\theta_i} \quad (4)$$

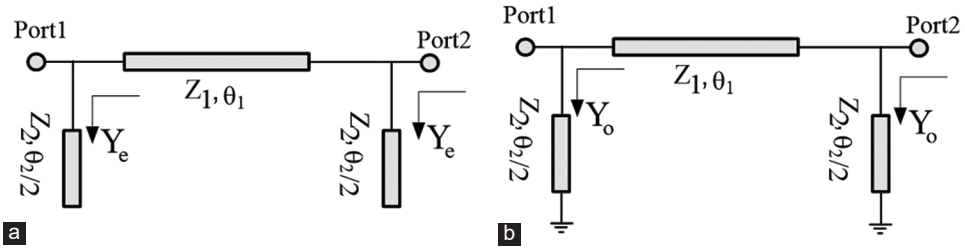

Fig. 5. Schematic diagram of the (a) even mode and (b) odd mode of the coupler.

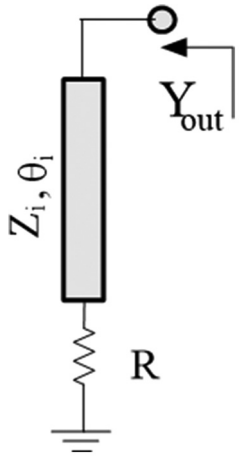

Fig. 6. Output admittance.

Therefore, Z_o is equal to:

$$Z_o = -jZ_i \tan \theta_i \quad (5)$$

If θ_2 in Fig. 5 is equal to 90°, therefore the $\theta_2/2$ is equal to 45°, and according to the cot(45°) = tan(45°) = 1, from equations (3) and (5), Z_e and Z_o can be obtained.

$$Z_e = -j\, Z_i \quad (6)$$

$$Z_o = j\, Z_i \quad (7)$$

In the even mode, the combined load of Z_{ein1} in Fig. 7 is:

$$Z_{ein1} = -jZ_2 \,||\, Z_0 = \frac{-jZ_2 Z_0}{Z_0 - jZ_2} \quad (8)$$

Equation (1) for θ_i = 90 degrees can be expressed as below:

$$Y_{in} = \frac{Z_i + jR\tan\theta_i}{RZ_i + jZ_i^2 \tan\theta_i}\Big|\theta_{i=90^\circ} = Y_{in} = \frac{R}{Z_i^2} \quad (9)$$

Therefore, the Z_{ein2} is obtained as:

$$Z_{ein2} = \frac{Z_1^2}{Z_{ein1}} \quad (10)$$

From (8) and (10):

$$Z_{ein2} = \frac{Z_1^2 (Z_0 - jZ_2)}{-jZ_2 Z_0} = \frac{j(Z_1^2 (Z_0 - jZ_2)}{(Z_2 Z_0)} \quad (11)$$

And the input impedance in the even-mode excitation is obtained:

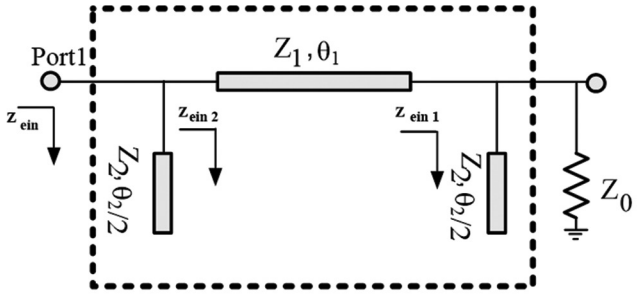

Fig. 7. Even mode analysis of the combiner.

$$Z_{ein} = Z_{ein2} \,||\, -jZ_2 \quad (12)$$

From (11) and (12), Z_{ein} is equal:

$$Z_{ein} = \frac{j\frac{Z_1^2 (Z_0 - jZ_2)}{Z_2 Z_0} \cdot (-jZ_2)}{j\frac{Z_1^2 (Z_0 - jZ_2)}{Z_2 Z_0} - jZ_2} \quad (13)$$

After some algebraic process, the equation (13) can be simplified as:

$$Z_{ein} = \frac{-Z_2 Z_1^2 \ (Z_2 + jZ_0)}{Z_0 \left(Z_1^2 - Z_2^2\right) - jZ_1^2 Z_2} \quad (14)$$

The odd-mode analysis of the combiner is obtained similarly.

In the odd mode, the combined load of Z_{oin1} in Fig. 8 is:

$$Z_{oin1} = +jZ_2 \,||\, Z_0 = \frac{Z_2 \ Z_0}{Z_0 \quad Z_2} \quad (15)$$

According to the quarter-wave length stub, the impedance of Z_{oin2} is obtained as follows:

$$_{oin2} \quad \overline{Z_{oin1}} \quad (16)$$

From (15) and (16):

$$_{oin} \quad \frac{Z_1^2 (\ Z_0 \quad jZ_2)}{Z_2 \ Z_0} = - \ \frac{Z_1^2 (\ Z_0 \quad jZ \ )}{Z_2 \ Z_0} \quad (17)$$

and the input impedance in the odd- mode excitation is obtained:

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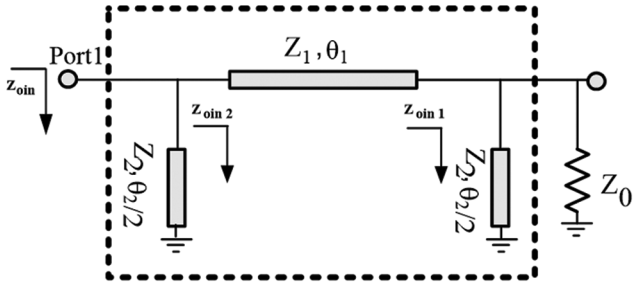

Fig. 8. Odd mode analysis of the combiner.

$$Z_{oin} = Z_{oin2} \,||\, jZ_2 \tag{18}$$

From (17) and (18), Z_{oin} can be obtained as follows:

$$\text{oin} \quad \frac{j\frac{Z_1\,(Z_0 \quad Z_2)}{Z_2\;Z_0}.(jZ\;)}{j\frac{Z_1\,(Z_0 \quad Z_2)}{Z_2\;Z_0}\quad j} \tag{19}$$

After some algebraic processing, equation (19) can be simplified as:

$$\text{oin} \quad \frac{Z_2 Z_1\;\;(Z_2 \quad jZ_0)}{Z_0\left(Z_2^{\,2} - Z_1^{\,2}\right) - Z_1^{\,2} Z_2} \tag{20}$$

From (14) and (20), according to the reciprocal and lossless network and from (Monzon, 2002), one answer to the dimensions of the coupler is:

$$Z_2 = Z_0 \tag{21a}$$
$$Z_1 = (/\sqrt{2}) \tag{21b}$$

In the proposed design, the RT/Duroid 5880 substrate is used, for which the quarter-wave transmission line (λ/4) is equal to 21 mm, W_{c1} = 2.54 mm, and W_{c2} = 1.56 mm; therefore, the layout of the applied coupler is obtained as shown in Fig. 9.

As shown in Fig. 9, the size of the designed coupler is 21 mm × 21 mm. The electromagnetic simulation (EM) results (S-parameters) of the coupler are shown in Fig. 10.

The load (R_M), which is seen by the main amplifier in Fig. 3b, can be derived as (Giofre, et al., 2013):

$$R_M = \frac{Z_1^{\,2}}{Z_0}\left(\frac{Z_2^{\,2}}{Z_1^{\,2} - Z_2^{\,2}}\right)^2 + \frac{I_A}{I_M}\frac{Z_1^{\,2}}{Z_2}\left(\frac{Z_2^{\,2}}{Z_1^{\,2} - Z_2^{\,2}}\right) \tag{22}$$

, where I_A and I_M are the fundamental currents of the auxiliary and the main amplifiers. In the proposed DPA, the main current (I_M) lags the auxiliary current (I_A) by 90°. When the auxiliary amplifier is turned off, the auxiliary current is zero (I_A = 0); then, according to (22), the R_M is described by (23) as below:

$$R_M = \frac{Z_1^{\,2}}{Z_0}\left(\frac{Z_2^{\,2}}{Z_1^{\,2} - Z_2^{\,2}}\right)^2 \tag{23}$$

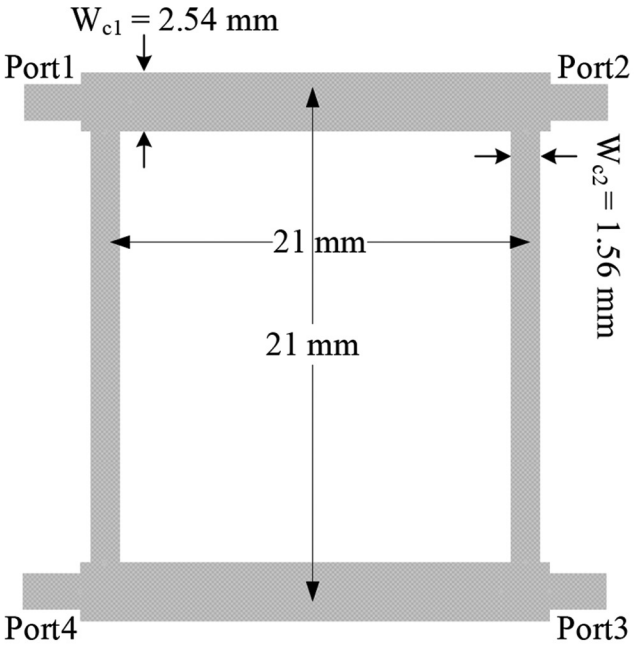

Fig. 9. Layout of the designed coupler.

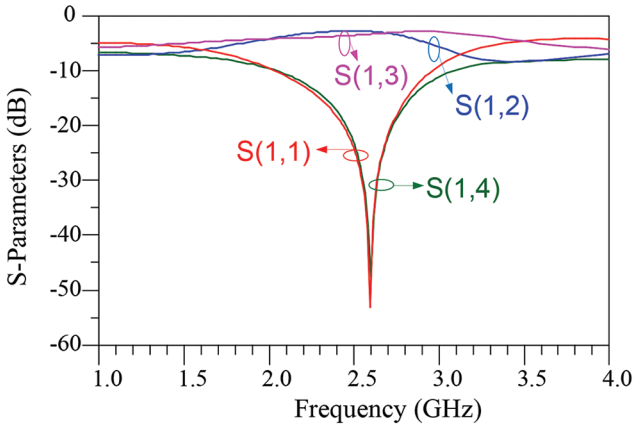

Fig. 10. The electromagnetic simulation results of the coupler.

In a particular case, by assuming

$$\left(\frac{Z_1}{Z_2}\right)^2 = \left(1 - \frac{Z_2}{2Z_0}\right) \tag{24}$$

The condition of (25) is obtained from (22), which this condition is necessary to have a 6 dB output back off (O.B.O) in DPA.

$$R_{M\,(IA\,=\,0)} = 2R_{M\,(IA\,=\,IM)} \tag{25}$$

In the proposed design according to (21), $Z_0 = Z_2$ = 50 Ω and Z_1 = (50/√2) Ω; therefore, the value of R_M is obtained from (26):

$$R_M = \left(100 - 50\frac{I_A}{I_M}\right)\Omega \tag{26}$$

In the proposed design, when the auxiliary amplifier is off (I_A= 0), according to (26), the main device load is about 100 Ω.

B. Load/Source Pull Analysis

The proposed PA is based on the Freescale's LDMOS transistor MW6S004N. The load pull and source pull simulations for the PA are performed in (Hayati and Roshani, 2014), and optimized impedances at the 2.6 GHz frequency range are listed in Table I.

C. DC Analysis

The design parameter values are listed in Table I. With the 2.8 V DC gate voltage of the main and 1.8 V, DC gate voltage of the auxiliary, the main and the auxiliary amplifiers are implemented using Class-AB and Class-C topologies, respectively.

D. Impedance Transformer Network

In this paper, an unequal-section impedance transformer is used in order to match the desired complex impedances at the input and output of the PA structure. Fig. 11 shows the block diagram of the output/input matching network of the designed PA.

According to Fig. 11 and Table I, the input impedance transformer network must transfer 50 Ω to the 7.5–12i Ω, and the output impedance transformer network must transfer 100 Ω to the 12–14i Ω. The value of Z_{s2} could be defined as:

$$Z_{s2} = Z_{i2}\frac{Z_s + jZ_{i2}tan(\theta_{i2})}{Z_{i2} + jR_s tan(\theta_{i2})} \quad (27)$$

where Z_s is the complex conjugate value of optimum source impedance (7.5–12j Ω).

The input impedance Zin could be defined as:

$$Z_{in} = Z_{i1}\frac{Z_{s2} + jZ_{i1}tan(\theta_{i1})}{Z_{i1} + jZ_{s2}tan(\theta_{i1})} \quad (28)$$

TABLE I
Design Parameters of the Proposed Doherty Power Amplifier

Parameter	Value
DC bias current (Main)	60 mA
DC supply voltage	28 V
DC gate voltage of the main	2.8 V
DC gate voltage of the auxiliary	1.8 V
Optimum load impedance	12-14i Ω
Optimum source impedance	7.5-12i Ω

To have a match at the input port, the following equation is necessary:

$$Z_{in} = Z_0^* = R_0 - jX_0 \quad (29)$$

The equation (28) can be rewritten as follows:

$$Z_x = Z_{i1}\frac{R_0 - jX_0 - jZ_{i1}tan(\theta_{i1})}{Z_{i1} - jR_0 tan(\theta_{i1})} \quad (30)$$

Equating (27) and (30) and combining $Z_s = R_s + j_X s$ resulted in:

$$Z_{i2}\frac{R_s + jX_s + jZ_{i2}tan(\theta_{i2})}{Z_{i2} + j(R_s + jX_s)tan(\theta_{i2})} = Z_{i1}\frac{R_0 - jZ_{i1}tan(\theta_{i1})}{Z_{i1} - jR_0 tan(\theta_{i1})} \quad (31)$$

Separating the real and imaginary parts of (31) resulted in:

$$(R_s Z_{i1}^2 - R_0 Z_{i2}^2)\ tan(\theta_{i1})tan(\theta_{i2}) = Z_{i1}\ Z_{i2}(R_s - R_0) + [Z_{i1}tan(\theta_{i2}) + Z_{i2}tan(\theta_{i1})] \times R_0 X_s \quad (32a)$$

$$R_0 R_s \times [Z_{i1}tan(\theta_{i2}) + Z_{i2}tan(\theta_{i1})] - Z_{i2}Z_{i1}^2 tan(\theta_{i1}) - Z_{i1}Z_{i2}^2 tan(\theta_{i2}) = Z_{i1}Z_{i2}\ (X_s) - X_s\ Z_{i1}^2 tan(\theta_{i1})\ tan(\theta_{i2}) \quad 32b)$$

Here, Z_{in} is equal to 50 Ω. Equations (32a) and (32b) are two equations with four unknown parameters (Z_{i1}, θ_{i1}, $Z_{i2,}$ and θ_{i2}). The approach in (Chen and Hamid, 1987) for a dual-frequency impedance transformer for complex impedances with two unequal sections can be used to find these parameters. One solution for equation (32) with a small size (less than a quarter wavelength), at 2.6 GHz frequency is: Zi1=39.9 Ω, θ_{i1}=36°, Z_2=12.5 Ω, θi_2=36.9°.

The schematic diagram of the two-section input impedance transformer network is depicted in Fig. 12a. As seen, the physical length of θ_{i1} is 8.32 mm, which equals 36°, and the physical width of Z_{i1} is 2.15 mm, which equals 39.9 Ω. The physical length of θ_{i2} is 8.4 mm, which equals 36.9°, and the physical width of Z_{i2} is 8.9 mm, which equals 12.5 Ω. The input impedance transformer network with analytically obtained values correctly transfers 50 Ω to the desired source impedance of the transistor at 2.6 GHz frequency, which is equal to 7.5–12j Ω. The validity of the results is confirmed by the ADS simulator, as shown in Fig. 12b. These parameters of the input impedance transformer network are obtained by the analytical method and confirmed with the ADS simulator.

According to Fig. 11 and Table I, the output impedance transformer network must transfer 100 Ω to 12–14j Ω. The value of Z_{L2} could be defined as:

$$Z_{L2} = Z_{o2}\frac{Z_L + jZ_{o2}tan(\theta_{o2})}{Z_{o2} + jR_L tan(\theta_{o2})} \quad (33)$$

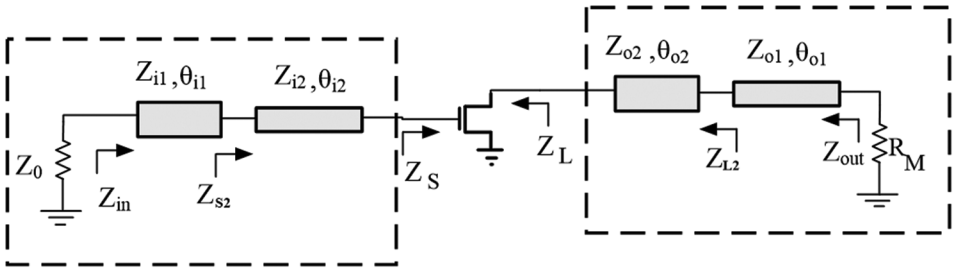

Fig. 11. Two-section impedance transformer network.

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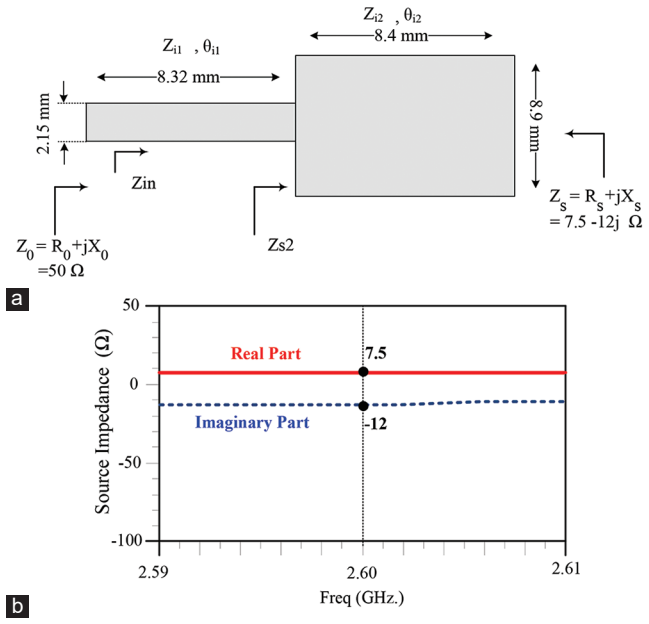

Fig. 12. The (a) two-section input impedance transformer network and (b) simulated results.

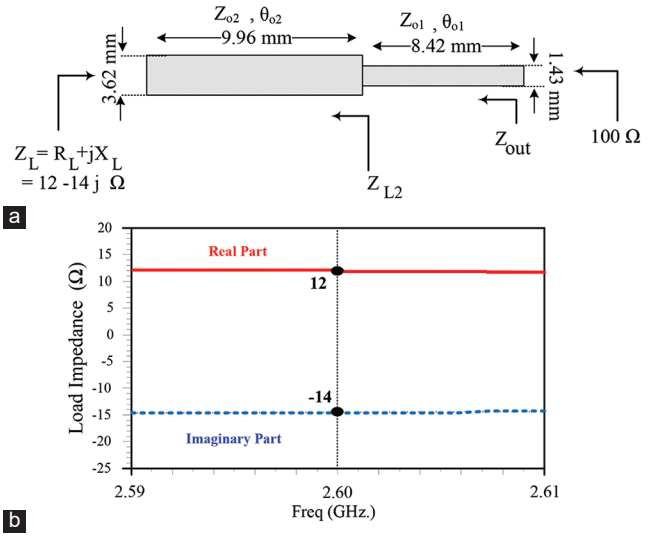

Fig. 13. The (a) two-section output impedance transformer network and (b) simulated results.

Where Z_L is the complex conjugate value of the optimum load impedance (12-14j Ω). Therefore, the output impedance Z_{out} is:

$$Z_{out} = Z_{o1}\frac{Z_{L2} + jZ_{o1}tan(\theta_{o1})}{Z_{o1} + jZ_{L2}tan(\theta_{o1})} \quad (34)$$

In a similar way, solving equations (33) and (34) has no unique answers for the unknown parameters (Z_{o1}, θ_{o1}, Z_{o2}, and θ_{o2}). These parameters of the output impedance transformer network are obtained with similar analysis and confirmed with the ADS simulator. One solution for these equations with a small size (less than a quarter wavelength at 2.6 GHz frequency is: Z_{o1}=52.9 Ω, θ_{o1}=36°, Z_{o2}=26.9 Ω, θ_{o2} =43.8°.

The schematic diagram of the obtained output impedance transformer network is shown in Fig. 13a. As seen, the physical length of θ_{o1} is 8.42 mm, which equals 36°, and the physical width of Z_{o1} is 1.43 mm, which equals 52.9 Ω. The physical length of θ_{o2} is 9.96 mm, which equals 43.8°, and the physical width of Z_{o2} is 3.62 mm, which equals 26.9 Ω. This impedance transformer network correctly transfers 100 Ω output impedance to the desired load impedance of the transistor at 2.6 GHz frequency, which is equal to 12–14j Ω, as shown in Fig. 13b.

The structure of the proposed DPA with two-section impedance transformer networks is shown in Fig. 14. The layout of the proposed DPA is designed based on the RT/Duroid 5880 substrate (relative permittivity of 2.2, thickness of 0.508 mm, and loss tangent of 0.0009). The size of the DPA is approximately 90.1 mm × 46 mm, equal to 1.02 λ × 0.52 λ. In addition, the layout of the typical DPA without a two-section network is shown in Fig. 14b, which indicates a larger size. In comparison with this typical DPA, the proposed design occupies 75% of the size, which shows a size reduction of 25%.

III. Results and Discussion

To assess the functionality of the designed DPA under steady-state conditions, large-signal simulations were conducted. Both the main and auxiliary devices operate using a drain bias of VDD = 28 V with 2.8 V gate voltage for the main amplifier and 1.8 V for the auxiliary amplifier. According to Fig. 15, the output power at the saturation point and P1dB compression point are calculated as 39.5 dBm and 38.5 dBm, respectively, which correspond to the input power levels of 29 dBm and 26.8 dBm. For the typical DPA, the 1 dB compression point corresponds to input and output power of 22.7 dBm and 34.7 dBm, respectively.

Fig. 16 shows the drain efficiency (DE) versus input power for the proposed DPA. The designed two-section network has increased the maximum efficiency from 38% to 45% in the proposed DPA. The maximum DE of 45% is obtained at the input power level of 29 dBm.

Fig. 17 shows the gain versus input power for the proposed DPA. An increment in the gain can be observed in the proposed DPA due to the applied two-section network. The maximum gain of 13.7 is obtained for the proposed DPA at the lower input power levels.

Fig. 18 presents the scattering parameters of the proposed Doherty amplifier near the operating bandwidth. The results confirm that the proposed DPA achieves good impedance matching at both input and output, along with high transmission efficiency, ensuring optimal performance within the operating frequency range of 2.6 GHz.

Fig. 19a and b show the DE and output power of the proposed Doherty amplifier versus frequency at two input levels of 29 dBm and 26.8 dBm, corresponding to the saturation point and 1 dB compression point. The results show that at the saturation point, the output power can reach

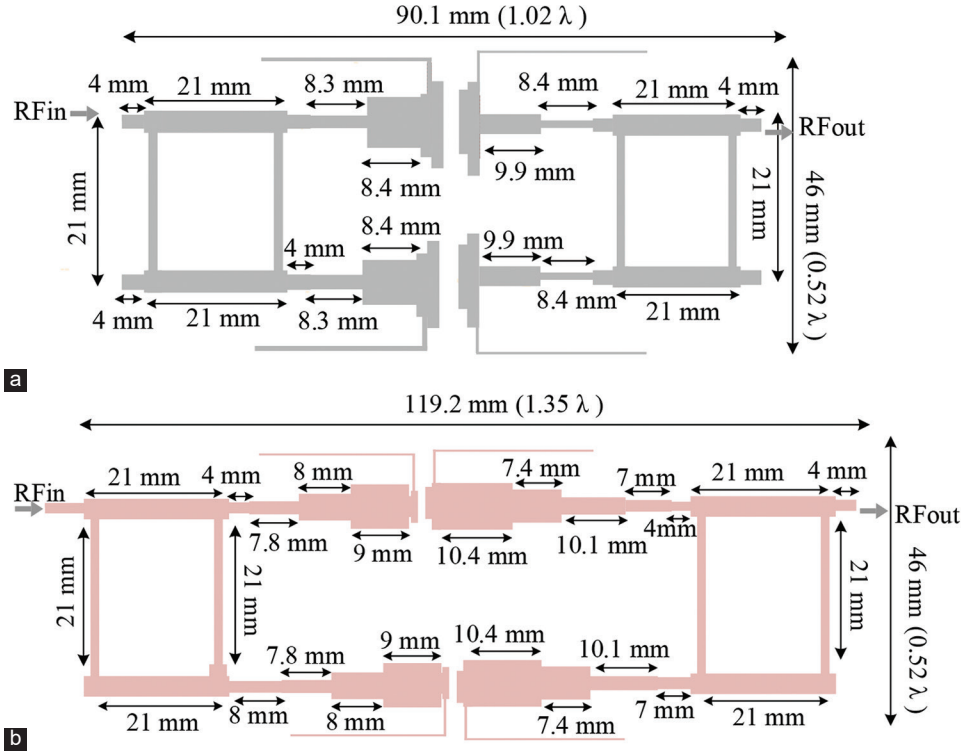

Fig. 14. Layout of the (a) proposed Doherty power amplifier with two-section impedance transformer networks and (b) typical Doherty power amplifier without two-section network.

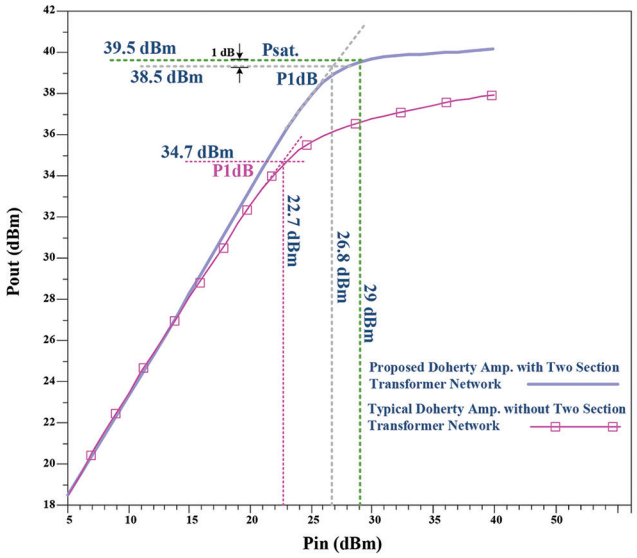

Fig. 15. Output power (P_{out}) versus input power (P_{in}) for the proposed Doherty power amplifier (circuit simulation results).

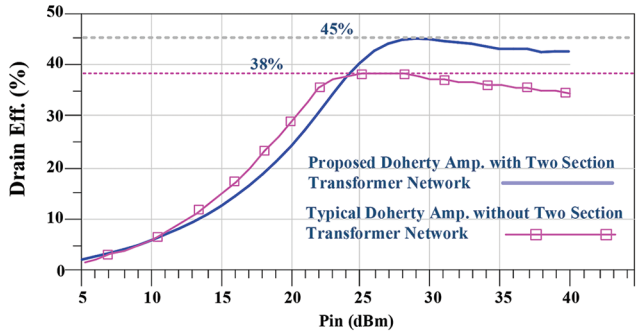

Fig. 16. Drain efficiency versus input power (P_{in}) for the proposed Doherty power amplifier (circuit simulation results).

39.5 dBm and the proposed DPA operates between 2.49 GHz and 2.67 GHz with DE of more than 30% and maximum efficiency of 45%. Furthermore, at the 1 dB compression point, the maximum DE and output power are 43.3% and 38.7 dBm. Moreover, in the operating bandwidth of 2.52 to 2.7 GHz, the DPA operates with more than 30% efficiency.

To verify the circuit-level simulations, the EM results at 2.6 GHz are provided, which closely align with the theoretical design and demonstrate consistent performance. The EM simulation results of the proposed DPA are shown in Figs. 20-22. According to the obtained EM simulation results, the output power at the 1 dB compression point is obtained equals to 37 dBm, corresponding to the input power level of 23.5 dBm. A 1.5 dB difference in the output power at the 1 dB compression point between circuit simulation (38.5 dB) and EM simulation (37 dB) is mainly due to the consideration of microstrip transmission line effects and coupler loss effects in the EM simulation model.

In addition, as shown in Figs. 21 and 22, the obtained DE reaches 45%, and the maximum gain of 15 dB is obtained for the proposed DPA.

In Fig. 23, EM simulation and circuit simulation results of the power added efficiency (PAE) parameter for the proposed

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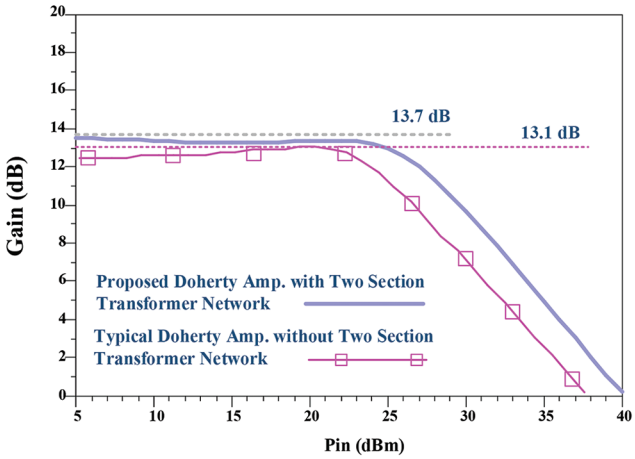

Fig. 17. Gain versus input power (P_{in}) of the proposed Doherty power amplifier (circuit simulation results).

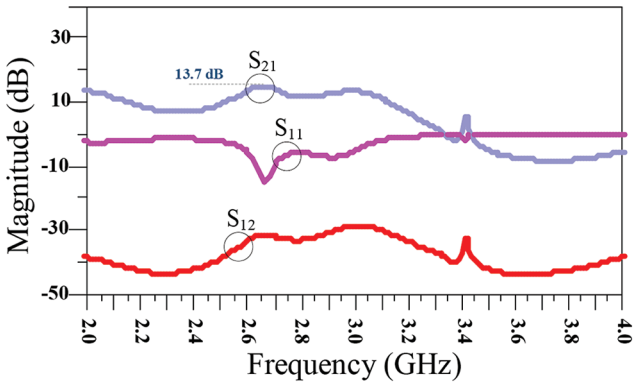

Fig. 18. The scattering parameters of the proposed Doherty amplifier (circuit simulation results).

DPA are depicted. Maximum 41% and 43% PAE are obtained in the EM simulation and circuit simulation, respectively. There is good agreement between EM simulation and circuit simulation results, which this agreement verifies the validity of the proposed DPA design.

Fig. 24 illustrates the DE of the proposed DPA as a function of output power at various frequencies. The obtained results show that the DPA achieves a peak DE of 45% at the saturation point for the operating frequency of 2.6 GHz. Furthermore, the results show that at a frequency of 2.6 GHz, best performance is obtained in 3-dB backoff from saturated output power. According to Fig. 24, it can be seen that in the bandwidth of about 180 MHz around the center frequency of 2.6 GHz, the DE remains above 30%.

To evaluate the linearity performance of the proposed Doherty amplifier, the IMD3, IIP3, and OIP3 parameters are shown in Fig. 25. A two-tone test is used in the EM simulation. The center frequency is 2.6 GHz and the tone spacing is considered equal to 20 MHz. In this test, the input power is swept over a wide range from −50 dBm to 10 dBm. The results show that the proposed DPA has an IIP3 value of 30 dBm and an OIP3 value of 42 dBm. According to these results, the proposed DPA has obtained desirable linearity.

A performance comparison of the designed DPA with other related Doherty amplifiers is shown in Table II. According to this table, the proposed DPA demonstrated good performance at the operating frequency, showing desirable specifications, compared to the other reported works. The proposed DPA achieves a high gain of 15 dB at a frequency of 2.6 GHz, a DE of 45%, and an output P1dB of 38.5 dBm, demonstrating competitive performance compared to other designs. The use of a two-section impedance transformer network and

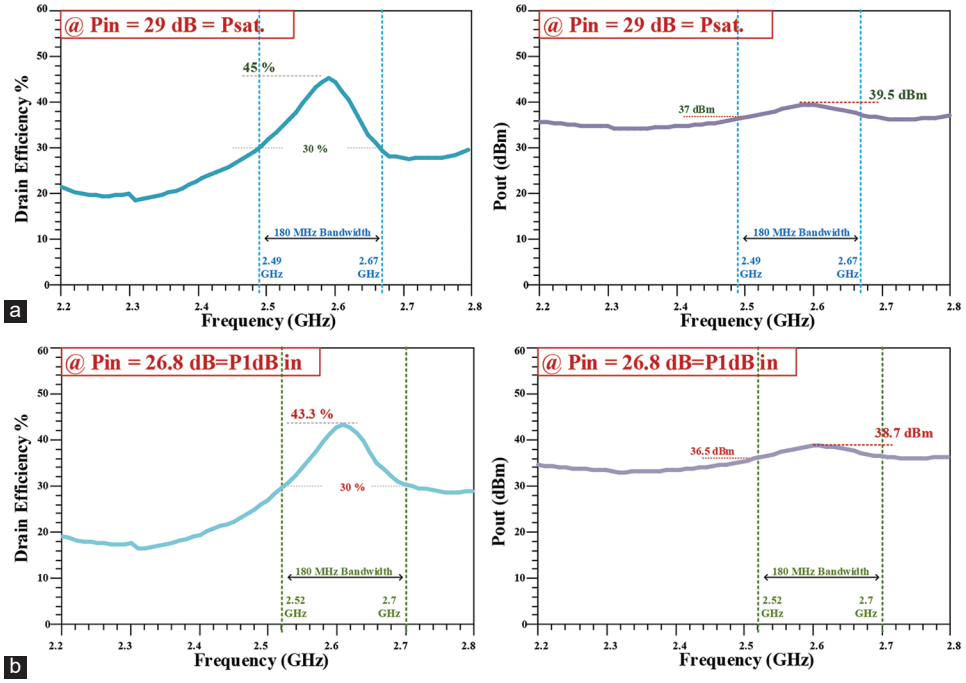

Fig. 19. Drain efficiency and output power of the proposed Doherty amplifier versus frequency. Simulated results at (a) saturation point with input power of 29 dB and (b) 1 dB compression point with input power of 26.8 dB (circuit simulation results).

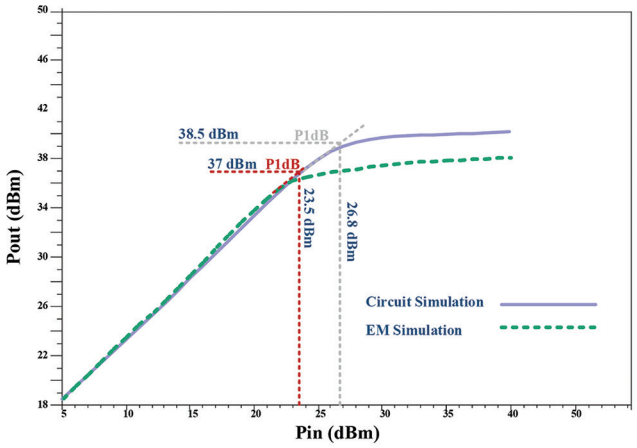

Fig. 20. Electromagnetic simulation and circuit simulation results of output power (P_{out}) versus input power (P_{in}) for the proposed Doherty power amplifier.

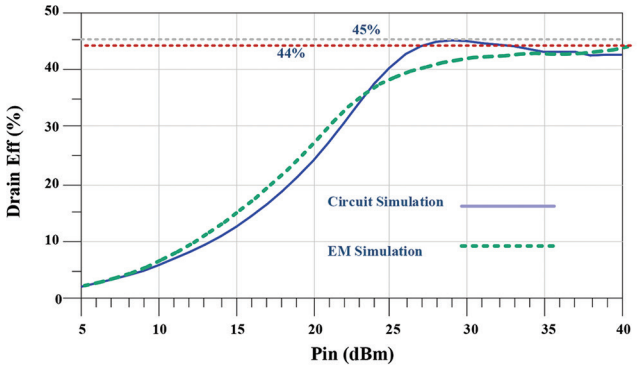

Fig. 21. Electromagnetic simulation and circuit simulation results of drain efficiency versus input power (P_{in}) for the proposed Doherty power amplifier.

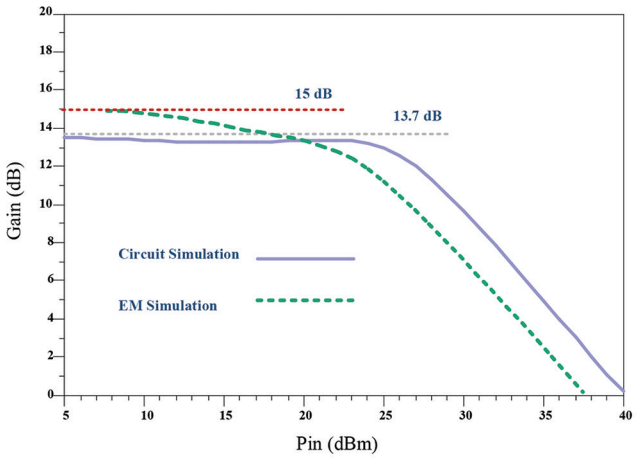

Fig. 22. Electromagnetic simulation and circuit simulation results of gain versus input power (P_{in}) for the proposed Doherty power amplifier.

a branch-line coupler allows for a compact layout size of 1.02 λ × 0.52 λ, smaller than other designs.

In comparison to other DPAs operating at similar frequencies, the proposed design strikes an excellent balance

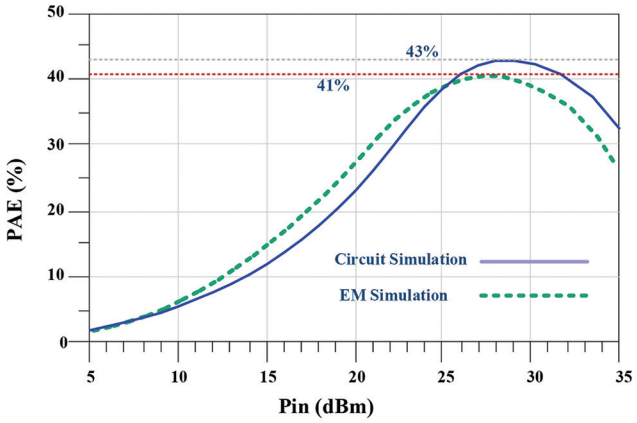

Fig. 23. Electromagnetic simulation and circuit simulation results of power added efficiency parameter versus input power (P_{in}) for the proposed Doherty power amplifier.

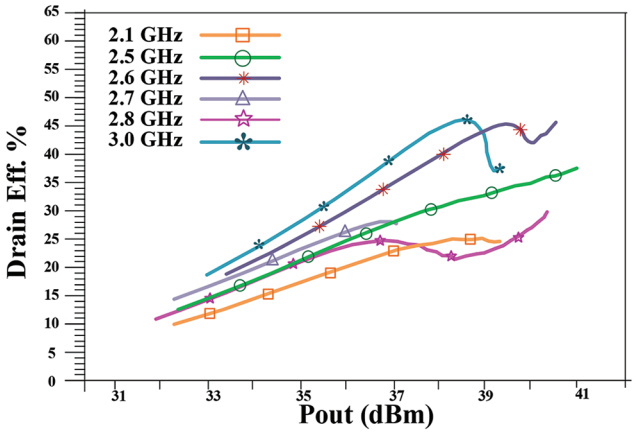

Fig. 24. Drain efficiency of the proposed Doherty amplifier versus output power for different frequencies.

between linearity and compactness. For instance, while some works achieve a higher maximum PAE, they have larger sizes and different device technology.

The improved PAE and wider operating bandwidth of the proposed DPA are mainly attributed to the combined effect of the branch-line coupler and the two-section impedance transformer. In conventional Doherty structures, the matching network is usually optimized around a narrow frequency region, which limits the load modulation performance away from the center frequency. In the proposed design, the branch-line coupler helps reduce mismatch and reflection losses at the combining and matching interface, whereas the two-section impedance transformer provides a smoother impedance transition over the target band. As a result, the effective load impedance seen by the carrier and peaking paths remains closer to the optimum value not only at peak output power but also in the backoff region. This improved load modulation behavior explains the observed enhancement in PAE and bandwidth compared with conventional reference structures. Therefore, the performance improvement is not only numerical, but also physically consistent with

TABLE II
PERFORMANCE COMPARISON OF THE PROPOSED DPA WITH OTHER RELATED DOHERTY AMPLIFIERS

Ref.	*f0* (GHz)	Gain	PAE (%)	P1dB Output	Size	Device	Substrate	Proposed Technique
(Chen, et al., 2011)	1.96	10 dB	50	38.5 dBm	Large-NR	MESFET CREE, CRF24010	NR	Dual-band T-shaped network; Coupled line network
(Kim, et al., 2010)	2.6	NR	NR	NR	Large-NR	GaN HEMT CREE CGH 40010	NR	Saturated amplifier
(Choi, Lim and Jeong, 2006)	2	10.5 dB	62	37 dBm	Large-NR	GaAs FET	εr=2.2, h=0.787 mm	Defected ground structure
(Moon et al., 2010)	2.6	7.4 dB	68	46.2 dBm	Large-NR	GaN HEMT CREE CGH 40045	NR	Knee voltage effect
(Zhou, Zhou and Chan, et al., 2022)	2.6	8.2 dB	52	41.2	0.89 λ×0.65λ	GaN HEMT CREE CGH 40010F	Rogers RO4003C, h=0.813 mm	Dual-mode impedance transformer
(Rubio, et al., 2017)	2.6	13 dB	43	41.3 dBm	1.47 λ× 1.76 λ	GaN HEMT CREE CGH 40010F	Taconic εr=3.5, h=0.76 mm	Bandwidth estimation
(Zhou, et al., 2019)	1.75	10 dB	60	41.8 dBm	0.94 λ× 1.25 λ	GaN HEMT CREE CGH 40010F	Rogers 4003C (εr=3.38, h=0.813 mm)	Harmonic injection network
(Li, et al., 2020)	3.17	9.1 dB	50	42 dBm	1 λ×1.16 λ	GaN HEMT CREE CGH 40010F	Rogers 5880 (εr=2.2, h=0.78 mm)	Modified Load Modulation Network
(Choi, 2023)	25 MHz	33 dB	57	35.7 dBm	NR	LDMOS	NR	Ultrasound Instrumentations
(Li, et al., 2019)	2.2-4.8	11.7 dB	51	NR	NR	GaN HEMT CREE CGH40006s	Rogers 5880 (εr=2.2, h=0.78 mm)	Reciprocal Gate Bias
(Xiao and Zhang, 2025)	3.5	14.4 dB	63	NR	NR	GaN HEMT CREE CGHV40030F	Rogers 4350B (εr=3.66, h=0.508 mm)	Asymmetric design, Independent Debugging Paths
Typical design	2.6	13.1 dB	37	34.7 dBm	1.35 λ× 0.52 λ	LDMOS MW6S004N	Rogers 5880 (εr=2.2, h=0.508 mm)	Typical branch-line coupler
This work layout	2.6	15 dB	41	37 dBm	1.02 λ× 0.52 λ	LDMOS MW6S004N	Rogers 5880 (εr=2.2, h=0.508 mm)	Two-section impedance transformer network; Branch-line coupler

NR: Not reported, f_0: Center Frequency, h: Substrate thickness, εr: Relative permittivity

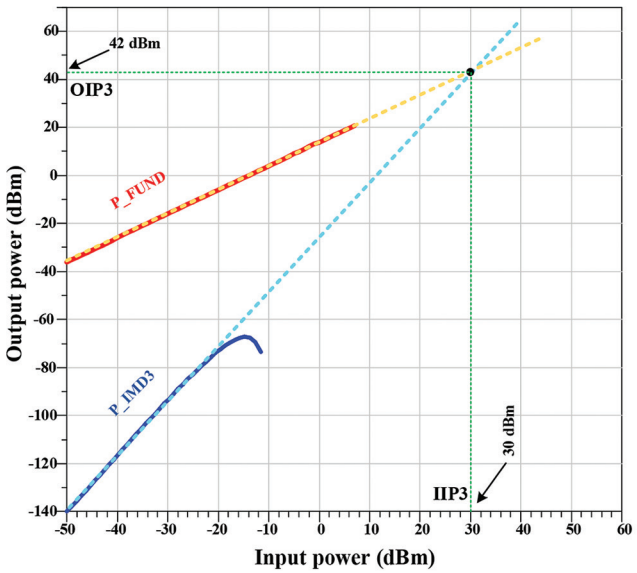

Fig. 25. The third-order intermodulation electromagnetic simulation result for the proposed Doherty power amplifier.

the proposed broadband matching and load modulation mechanism.

IV. Conclusion

In this paper, a DPA design has been presented. Freescale LDMOS transistors are used for both the main amplifier operating in Class-AB and the auxiliary amplifier operating in Class-C. In the proposed structure, a branch-line coupler is employed instead of the conventional output combiner, and a compact two-section impedance matching network is used to achieve proper impedance transformation. The proposed DPA operates at a center frequency of 2.6 GHz. The results show that the amplifier achieves a maximum gain of about 15 dB. The DE reaches 45% with an input power of 29 dBm. At the 1-dB compression point, the output power is about 38.5 dBm with an input power of 26.8 dBm. The reported results are based on ADS simulations and layout-level validation. The results show high efficiency, small size, and desirable linearity for the proposed amplifier. The obtained results confirm the proposed DPA's suitability for high-efficiency and high-linearity requirements in modern communication systems.

Acknowledgment

The authors extend their appreciation to the Deputyship for Research and Innovation, Ministry of Education in Saudi Arabia, for funding this research work through the project number (IF2/PSAU/2022/01/21241).

Data Availability Statement

All the material used in the study is mentioned in the article.

Conflicts of Interest

The authors declare no conflict of interest.

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